REMARKS

Claims 1-21 and 36-44 are all of the claims pending in the application. New claims 39-44 have been added to more completely define the invention.

Applicant again gratefully acknowledges the Examiner's indication in the December 4, 2002, Office Action, that claims 6, 11, and 13 would be allowable if rewritten in independent form. Claims 6 and 11 have been rewritten in the March 4, 2003, Amendment to place each of claims 6, 11, and 13 in condition for immediate allowance.

The prior art rejection of Claims 1-21 and the 35 U.S.C. §112, second paragraph, rejections of claims 1-17 as being "indefinite", are believed to have been overcome by the March 4, 2003, Amendment.

Additionally, with respect to the prior art rejections, in the December 4, 2002 Office Action, these rejections are respectfully traversed in view of the discussion in the March 4, 2003, Amendment, incorporated herein by reference, as well as in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment. The attached page(s) is captioned "**Version with Markings to Show Changes Made**"

It is noted that the claim amendments herein are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., see independent claim 1), is directed to a method (and resultant structure) of forming a semiconductor device, which includes forming a metal-back-gate over a substrate and a metal back-gate, forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species, and providing an intermediate gluing layer between the substrate and the metal back-gate to enhance adhesion between the substrate and the metal back-gate. Such features allow the problems of the conventional methods to be overcome.

That is, laminating a thin metal layer (e.g., tungsten (W)) between silicon-based materials such as a gate oxide and a buried oxide is a key step to making substrates for double-gate devices with a metal back-gate. Because of its flexibility with all kinds of materials, even if the materials are polycrystalline, amorphous, or single crystalline but with very different lattice mismatch, wafer bonding is a promising approach to make this multilayer structure.

However, for the bonding process, after the room-temperature joining step, a thermal treatment at 1100 °C is commonly used to enhance the bonding strength. Due to the weak adhesion at the interface between metals and, for example, silicon oxide as a result of their chemical and physical incompatibility such as thermal mismatch, the stacked layers are very likely to disintegrate during the high temperature bonding anneal in the form of delamination at weak interfaces.

A key feature of the method of the present invention is to use an intermediate "gluing" layer to enhance adhesion between multi-layers especially two layers with very different chemical and physical properties.

With the above and other unique and unobvious aspects of the present invention, substrates can be made for double-gate devices with a metal back-gate including using wafer

bonding, and, despite after the room-temperature joining step, a thermal treatment at 1100°C is used to enhance the bonding strength.

That is, even with chemical and physical incompatibility of layers, the stacked layers are not likely to disintegrate during the high temperature bonding anneal, and delamination will not occur at the interfaces.

Thus, the present invention resolves the above-mentioned and other problems of delamination between, for example, W and low temperature oxide (LTO) during bonding anneal by improving the adhesion between these two incompatible materials with several innovative processes.

None of the cited references, either alone or in combination, teaches or suggests such a combination of features.

III. THE PRIOR ART REJECTIONS

As discussed in the March 4, 2003, Amendment, the claimed invention differs from each of the cited references, either alone or in combination, by the recitation of the intermediate "gluing" layer to enhance adhesion between multi-layers especially two layers with very different chemical and physical properties.

As mentioned above, the present invention resolves the above-mentioned and other problems of delamination between metals and , for example, a low temperature oxide (LTO) during bonding anneal by improving the adhesion between two incompatible materials with several innovative processes.

Thus, the claimed invention is patentable over all of the prior art of record, as discussed below for the record.

A. The Linn et al. Reference

Linn et al. discloses a bonded wafer processing with metal silicidation.

However, Linn et al. is completely irrelevant to the claimed invention, for all of the reasons discussed in the March 4, 2003, Amendment.

Additionally, Applicant points out that Linn et al. (e.g., see col. 6, lines 55-62 and col. 7, lines 3-35) teaches a method of bonding Tungsten (1000 Å) on polysilicon (500 Å) by placing a drop of oxidizing aqueous solution of HNO_3 and H_2O_2 solution on polysilicon. The drop is 20% by volume a 67% HNO_3 solution and 80% by volume a 30% H_2O_2 solution. Thereafter, heating occurs to 900°C in a 2- 6 hour-furnace cycle with an oxidizing ambient.

This reaction achieves tungsten silicide, and drives polysilicon to form silicon oxynitride, and a bonded backgate is achieved. The reactions are basically :

$W + 2Si \text{ -----> } WSi_2$

$Si + HNO_3 + H_2O_2 \text{ -----> } Si_xO_yN_z + H_2O + O_2$

$WSi_2 + HNO_3 + H_2O_2 \text{ -----> } Si_xO_yN_z + W_aO_bN_c + H_2O + O_2$

Thus, Linn teaches an ex-situ method to form a bonded W backgate which includes sputtering (PVD) W, and in which a passivation layer is a W layer (e.g., see Figures 5A and 5B).

In complete and fundamental contrast, the inventive method teaches forming a metal backgate which comprises metal (e.g., W in the exemplary embodiment) + an intermediate layer (e.g., in the exemplary embodiment, W-Si-N), (a so-called "gluing layer").

This "intermediate layer" is grown preferably by in-situ UHV CVD growth of W-Si-N , which is a thin atomic structure, will have minimal addition of stress (e.g., thickness is a large factor in increasing stress). This idea can be used in any metal if the metal forms a

metal - Si - N structure. Thus, the inventive backgate comprises metal + intermediate layer of metal-Si-N.

There are some potential problems in Linn's teachings which clearly teach away from the claimed invention. For example, based on Linn's proposed chemical reactions, the drop (HNO_3 + H_2O_2) to achieve bonding of tungsten and Si forms water vapor and oxygen gases after annealing at 900°C for 2 to 6 hours. This water vapor and oxygen gas will break through the top Si, oxide, polysilicon (e.g., see Fig 5A) in the form of bubbles (which were encountered by the present inventors in some of their experiments).

Additionally, in Linn et al., it is noted that tungsten is highly stressed, and thick $W_aO_bN_c$ is even higher stressed in combination with a thick silicon oxynitride. During the furnace annealing at 900 °C, these films can buckle up and peel off from the surface. It has been observed by the present inventors as well as by many other investigators.

Thus, even if Linn et al. bears some superficial similarities with the claimed invention, the principle of operation and fabrication of Linn et al. are completely different from the claimed invention, and thus Linn et al. fails to teach or suggest the claimed invention.

Indeed, in the invention defined by independent claim 1, an intermediate gluing layer is provided on the passivation layer to enhance adhesion between the metal back-gate and the substrate.

In contrast, in Figures 5A-5B of Linn et al., layer 517 is not the "intermediate gluing layer" of the claimed invention and clearly fails to teach or suggest the same. That is, the intermediate gluing layer of the claimed invention is for enhancing adhesion between the metal back-gate and the substrate. The polysilicon layer 517 performs no such function, nor is such disclosed or suggested by Linn et al.

Indeed, nowhere does Linn et al. teach or suggest that the polysilicon layer is 517 is an

intermediate gluing layer provided on a passivation layer for enhancing the adhesion between the tungsten layer and the substrate of Linn et al.

Thus, Linn et al. fails to teach or suggest "*[a] method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate", as defined by independent claim 1.

Independent claim 18 is patentable for somewhat similar reasons in that no passivation layer (if any) formed in Linn et al. is for enhancing adhesion between the substrate and the metal back-gate.

Therefore, Linn et al. fails to anticipate or, for that matter, render obvious the claimed invention defined by claims 1-4, 7-8, 12, and 14-18.

B. The Secondary References to Maiti et al. and Chan et al.

Regarding the rejection of claim 5 and the rejection of claims 9-10 and 19-21, the Examiner additionally relies on Maiti and Chan et al., respectively, for making up for the deficiencies of Linn et al. Applicant respectfully disagrees for all of the reasons discussed in the March 4, 2003, Amendment, incorporated herein by reference.

Additionally, Maiti et al. teaches a method of forming semiconductor device including providing substrate and depositing dielectric and metal gate layer.

In contrast, as mentioned above, the inventive method teaches a way to form a metal backgate which comprises metal (e.g., W in an exemplary, nonlimiting embodiment of the present invention) + intermediate layer (e.g., W-Si-N in a nonlimiting embodiment of the

present invention) (the "gluing layer"). This "intermediate layer" is grown by in-situ UHVCVD growth of W-Si-N , which is a thin atomic structure, will have minimal effect of stress (e.g., thickness is a large factor of increasing stress). This idea can be used in any metal if metal forms metal - Si - N. Thus, the inventive backgate comprises metal + intermediate layer of metal-Si-N.

Thus, even assuming arguendo that Maiti et al. would have been combined with Linn et al., Matti et al. teaches the forming of front gate, and does not teach or suggest the forming of metal backgate in the substrate.

Additionally, regarding the rejection of claims 9-10 and 19-21, Chan et al. teaches a method of bonding Si substrate very carefully. Their heating cycle is very carefully designed (Col 4, line 49 to Col 5, line 3) to prevent or minimize any stress and bubbles at the bonding interface. There would have been no reason, motivation or suggestion, absent hindsight, to combine Chan et al. with Linn et al., especially considering that, as described above, in Linn et al., the tungsten is highly stressed, and thick $W_aO_bN_c$ is even higher stressed in combination with a thick silicon oxynitride. Thus, during the furnace annealing at 900 °C, these films can buckle up and peel off from the surface. Hence, Chan et al. and Linn et al. are at odds with each other.

The claimed invention teaches the formation of metal backgate with an intermediate layer which will minimize the stress at the interface.

Thus, even if the references would have been combined, the claimed invention would still not have been produced.

Thus, there is no teaching or suggestion of "*providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate*", as defined by independent claim 1.

Hence, claims 5, 9-10, and 17-19 would not have been rendered obvious by the

Examiner's urged combinations of Linn et al. in view of either of Maiti et al. or Chan et al.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "*[a]" method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate (emphasis Applicant's), as defined by independent claim 1.

Further, there is no teaching or suggestion of "*[a] method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate; and

providing a passivation layer between said substrate and said metal back-gate to enhance adhesion therebetween (emphasis Applicant's), as defined by independent claim 18.

Finally, there is no teaching or suggestion of "*[a] method of forming a semiconductor substrate, comprising:*

growing a gate oxide on a silicon-on-insulator (SOI) material;

depositing a refractory metal onto said gate oxide; and

forming a passivation layer on said refractory metal" (emphasis Applicant's), as defined by independent claim 19.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Linn et la., Maiti et al., and Chan et al. fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-21 and 36-41, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 3/20/03

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Renzo Rochegianni, Group Art Unit 2825 at fax number (703) 872-9318 this 20th day of March, 2003.

Sean M. McGinn
Reg. No. 34,386

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please add the following new claims:

--39. The method of claim 1, wherein said providing said intermediate gluing layer on said passivation layer comprises growing said intermediate layer by in-situ ultra high vacuum chemical vapor deposition (UHV CVD) growth of metal-Si-N.

40. The method of claim 39, wherein said metal comprises tungsten.

41. The method of claim 18, wherein said providing said passivation layer comprises growing said passivation layer by in-situ ultra high vacuum chemical vapor deposition (UHV CVD) growth of metal-Si-N.

42. The method of claim 41, wherein said metal comprises tungsten.

43. The method of claim 19, wherein said providing said passivation layer comprises growing said passivation layer by in-situ ultra high vacuum chemical vapor deposition (UHV CVD) growth of metal-Si-N.

44. The method of claim 43, wherein said metal comprises tungsten.